B.Tech. (Third Semester) Examination, 2013

(ELECTRONIC DEVICES & CIRCUITS)

SECTION A

1. (a) Diode current equation is given by $I = I_0(e^{V/\eta V_T} - 1)$

(b) Efficiency of full wave Rectifier is 81.2 %

(c) NPN transistor is prefferred over PNP because electrons are majority carriers in NPN transistor and it has larger mobility as compared to holes.

(d) Emitter current in CB configuration

$I_C = \alpha I_E + I_{CBO} \Rightarrow I_E = \dfrac{I_C - I_{CBO}}{\alpha}$

(e) Trans conductance g_m is given by

$$g_m = \alpha_0 \frac{\partial I_E}{\partial V_E} = \frac{\alpha_0}{r_e} = \frac{\alpha_0 I_E}{V_T} = \frac{|I_C|}{V_T}$$

(f) In order to determine h_{fe} and h_{ie} parameter of transistor $V_C = 0$, collector is shorted to emitter.

(g) In wien bridge oscillator generated freq. is

$$f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}, \quad f = \frac{1}{2\pi RC}$$

(h) for LC tuned circuit $L = 29.3\ MH$, $C = 450\ PF$

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{29.3\times10^{-6}\times450\times10^{-12}}} = 1.386\ MHz.$$

(i) $V_0 = -\dfrac{1}{CR_f}\int V_i\,dt$. (Integrator o/p)

(j) TRUE

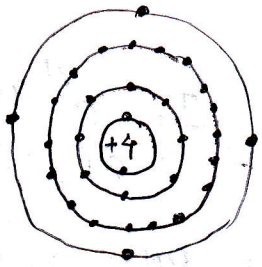
SECTION B

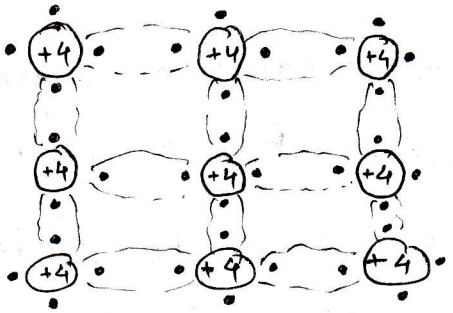
Ans 2 (a): what did you mean by intrinsic semiconductor? what are the disadvantages of them? How to the disadvantage can be removed

Ans: The conductivity of semiconductor depends on the concentration of free electron. For semiconductor i.e Ge and Si in pure form, the valence electrons are of

free to move but are bound between two adjacent ion

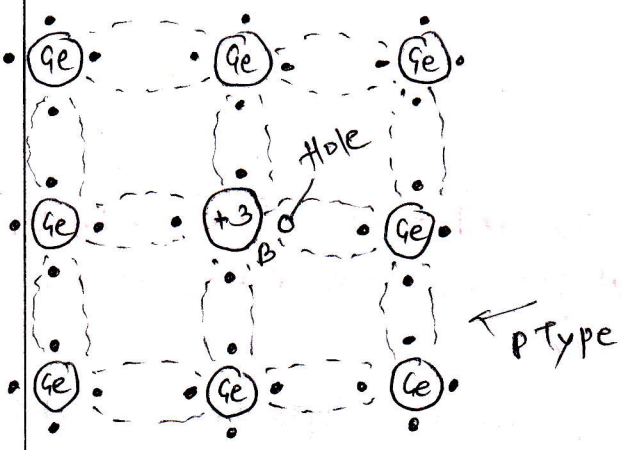
$_{32}Ge \longrightarrow 1s^2, 2s^2, 2p^6, 3s^2, 3p^6, 3d^{10}, 4s^2, 4p^2$

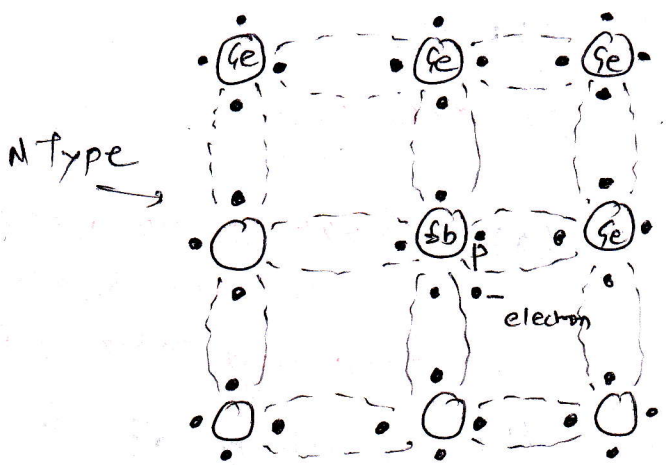




The dashed line shows covalent bond between atoms. each of the valence electron of Ge atom is shared by, valence electron of neighbouring four Ge atom as shown one above. This results in valence electrons being highly bound to the nucleus. Hence inspite of the availability of four valence electrons the crystal has low conductivity or we can say at 0°K intrinsic semiconductor or pure semiconductor behave like insulator. At room temperature there will be availability of free electron because electron will get 1.1 eV of energy from room temp and breaks the covalent bond and free electrons will be available for conduction of current.

Now to increase the conductivity of intrinsic semiconductors some impurities are added which are either trivalent impurity like B, Al, Ga, In or pentavalent impurities like P, As Sb, Bi with pure semiconductor (Ge or Si) which results in P type or N type of Extrinsic semiconductor which results in increased conductivity as explained by fig below



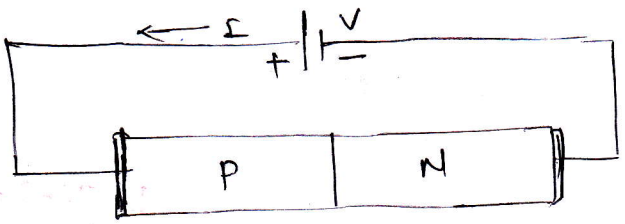


from the fig shown above trivalent impurity B is added

to pure Ge. Boron has 3 valence electron in its outer shell which makes ~~four~~ 3 covalent with 3 valence e⁻ of Ge atom but in fourth covalent bond there is a vacancy for an electron which is known as HOLE and is free to move and acts as a carrier for P type semiconductor. Each impurity atom added results in one free hole, therefore conductivity of semiconductor has been increased with hole as majority carriers due to addition of doping. Similarly pentavalent impurity can be added to pure semiconductor and results in N type semiconductor with electron as free carrier and causes ~~cost~~ increase in conductivity.

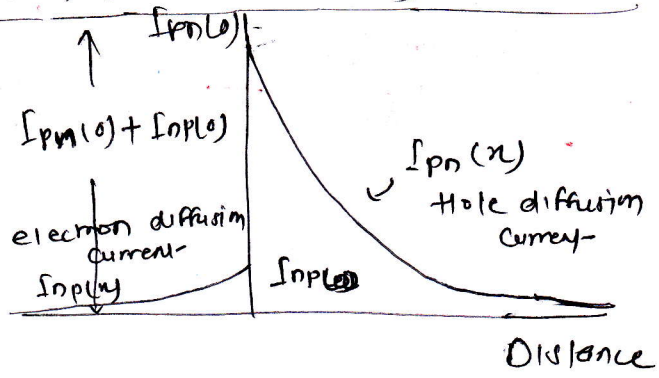
Q/2 (b) Explain Current components in PN diode in detail.

Ans In a diode when forward bias is applied holes are injected into n side and electrons into p side



Hence the current can be considered only due to majority carrier drift and minority current (is only due to) diffusion The hole diffusion current in the N type material I_{pn} decreases exponentially as shown (with distance)

The doping is assumed to be non identically, acceptor concentration is much larger compared to donar concentration therefore I_{pn} (hole diffusion current) is much larger than electron diffusion current. So the total diode current in a diode can be assumed to be the addition of the two currents



and is given by $I = I_{pn}(0) + I_{np}(0)$

The total diode current is given by $I = I_o(e^{V/V_T} - 1)$

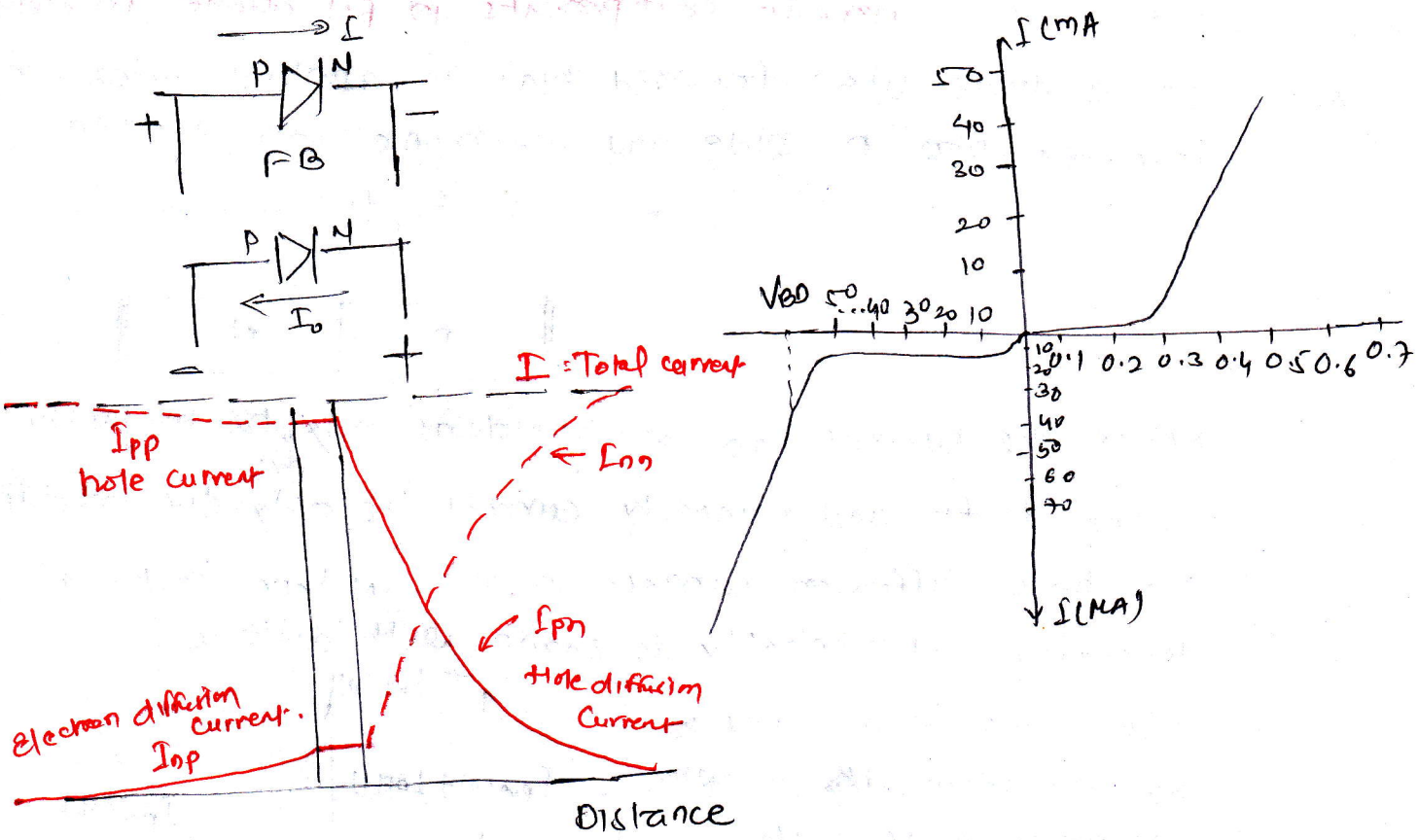
where I_o = Reverse saturation current

V = Applied voltage

V_T = Voltage equivalent of temperature

+ve voltage applied indicated forward bias, above equation hold good fore -ve voltage for reverse biasing condition of the diode. For reverse voltage larger than V_T ($\approx 26mV$) $I \approx -I_o$ and is called reverse saturation current and it depends only on temperature because it results due to thermally generated carriers.

Above diode current equation may be plotted as shown below

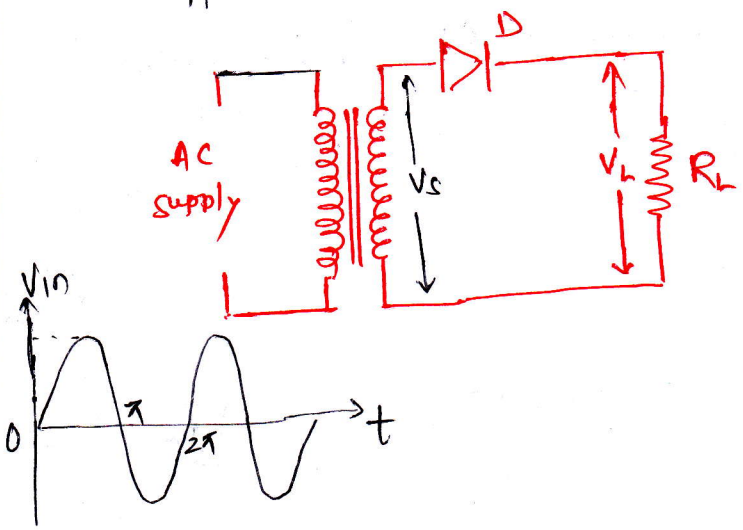


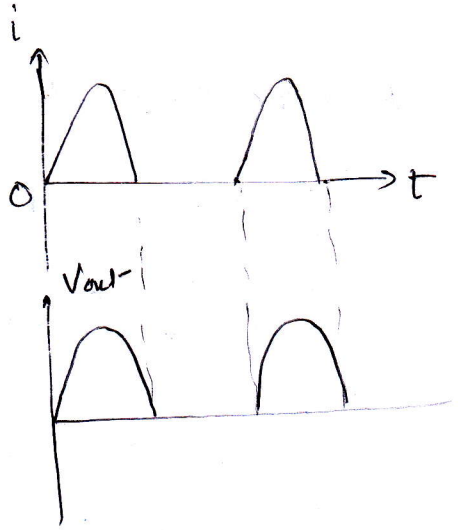
9/2 (C) Explain operation of HWR and compare it with FWR. Also derive for average value and RMS value for HWR waveform.

Ans:- Rectifier is a device which converts alternating waveform to unidirectional. A simple PN junction which acts as switch. when forward biased it behaves like ON switch and when reverse biased, acts as OFF switch.

Half Wave Rectifier:-

A half wave Rectifier is device such as diode which is capable of converting a sinusoidal input waveform (average value = 0) into unidirectional output waveform with non zero o/p waveform.

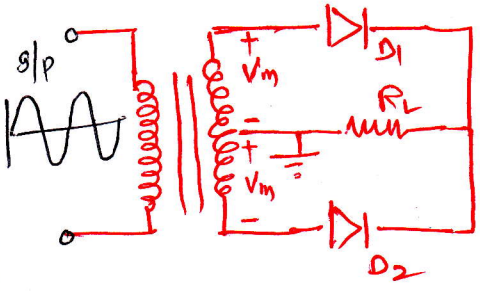




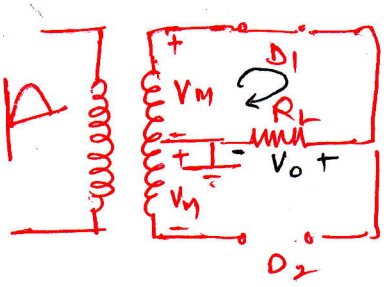
For +ve half cycle of o/p waveform diode P side is connected to +ve and N side to -ve and diode acts as forward biased and current flows from load R_L downwards and load voltage is +ve.

Again for next half cycle P side of diode is connected to -ve terminal of supply and N side is connected to +ve terminal, diode acts as reverse biased and will be opened and o/p is equal to zero and the o/p repeated for next +ve half cycle.

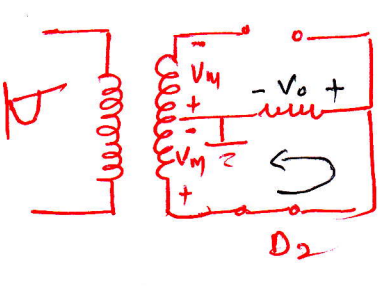
Full Wave Rectifier



+ve Half



-ve half



Full wave Rectifier circuit is shown in figure. For +ve half diode D_1 is forward biased and acts as short circuit and current from load R_L is right to left. Similarly for -ve half of o/p waveform diode D_1 is RB and D_2 is FB and acts as short with D_2 open as shown. direction of current from load R_L is again from right to left. So Input current is alternating but o/p current remains unidirectional. hence above circuit acts as rectifier.

Comparison o/p waveforms HWR FWR

Average value of o/p current (HWR)

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i\,d\theta = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin\theta\,d\theta$$

$$= \frac{1}{2\pi}\int_0^{\pi} I_m \sin\theta\,d\theta$$

$$= \frac{I_m}{2\pi}\left[-\cos\theta\right]_0^{\pi} = I_m[1+1]$$

$$\boxed{I_{AVG} = I_{DC} = \frac{I_m}{\pi}}$$

RMS value (HWR)

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2\,d\theta}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\theta\,d\theta}$$

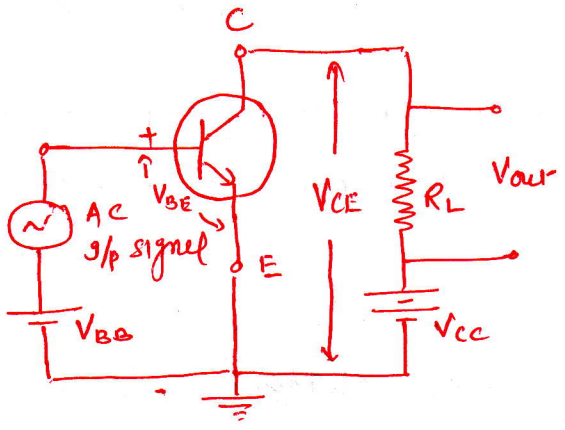
$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi} \frac{1-\cos 2\theta}{2}}$$

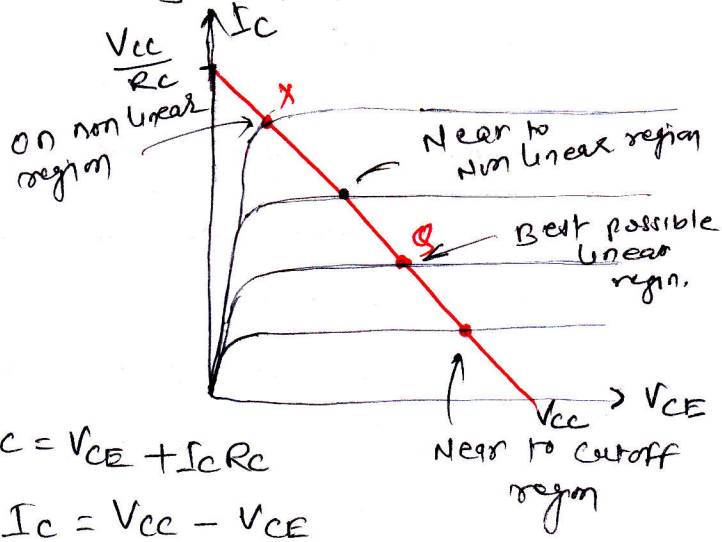
$$= \sqrt{\frac{I_m^2}{2\pi}\cdot\frac{1}{2}\left[\theta\right]_0^{\pi} - 0}$$

$$\boxed{I_{RMS} = \sqrt{\frac{I_m^2}{4\pi}\cdot\pi} = \frac{I_m}{2}}$$

Q/3: (a) What are the needs for biasing voltage for a transistor acting as an amplifier? Give the CE amplifier circuit and explain its operation for voltage gain.

Ans:- For most of the application transistors are required to operate as linear amplifier to amplify i/p voltage. To achieve this i.e. to operate the transistor in the linear region shown in figure below biasing voltage are needed. for proper selection of operating point (Q point), proper biasing i.e. i.e. proper selection of emitter to base voltage and collector to base junction is required. If transistor is not biased properly it would work inefficiently and produce distortion.





$$V_{CC} = V_{CE} + I_C R_C$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

constant

When $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C}$

when $I_C = 0$, $V_{CE} = V_{CC}$

} used to draw load line

The CE amplifier circuit is shown above. Biasing supply is needed to operated transistor (NPN) in linear region. The weak signal to be amplified is applied at emitter base junction and o/p is taken at load R_L connected in series with V_{CC}. For amplification transistor should act in active region i.e. E-B junction FB and CB junction reverse biased for whole duration of application of i/p signal which is achieved by batteries V_{BB} and V_{CC}. Now i/p circuit is FB

and hence has low resistance and small voltage change ΔV_{in} in input signal (AC i/p signal) causes very large change in I_E and hence I_C because of transistor action. This increased collector current flows through high load resistance and generate a large voltage across it. The change in output voltage across load R_L may be many times the change in i/p. $A = \frac{\Delta V_o}{\Delta V_{in}}$.

Let $R_L = 10K$. and $\Delta V_{in} = 0.1V$ cause a change in I_E of 0.05 mA. This change in I_E causes, I_C to to change depending upon β of transistor. for ex. $\beta = 50$, $I_C = \beta I_B = 2.5mA$

o/p voltage $= I_C R_L = 2.5 \times 10^{-3} \times 10 \times 10^3 = 25.0V$, $A_v = \frac{25.0}{.1} = 250$

Q/3 (b) What did you mean by Early effect ? explain its three consequences in the operation of a transistor.

Ans: We know that for transistor to operate in active region EB junction is FB and CB junction is RB. The width of the depletion region of diode changes with applied bias. As EB junction is FB, barrier width at emitter junction will be negligible and as CB junction is RB biased, barrier width will be more at I_C. Now if reverse biasing applied at I_C is increased. As we allready know base of transistor is lightly doped (p type for NPN) and collector is moderatly doped (> base). depletion region width increase because of applied reverse bias penetrate more towards lightly doped region i.e. base because.

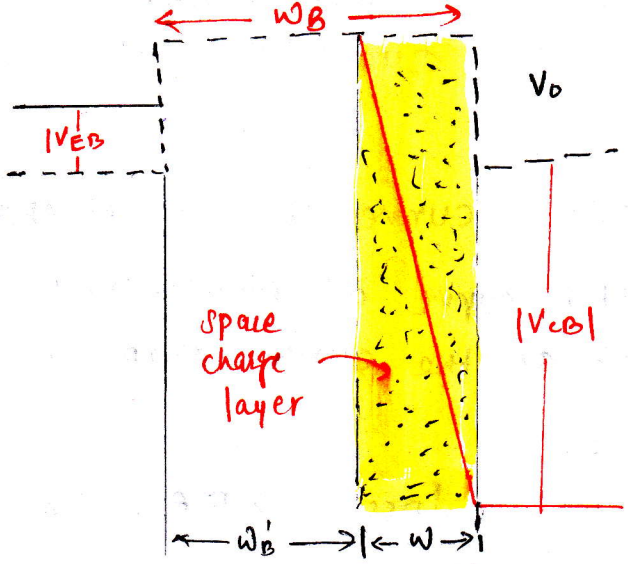
$$\underset{\text{volume}}{N_A x_p A} = \underset{\text{volume}}{N_D x_n A}$$

charge neutrality maintained

$$\frac{N_A}{N_D} = \frac{x_n}{x_p}$$

As $N_A < N_D$, $x_n < x_p$

x_p is barrier penetration in base.



As per the explanation given the depletion layer penetrates more into base than collector. Hence collector depletion region is neglected. If the base width is W_B, then effective electrical base width is $W_B' = W_B - W$ due applied reverse bias at CB junction. This modulation of effective base width by collector voltage is known as Early effect. The decrease in W_B' with increase in reverse collector voltage has three consequences

1. Base width is decreased hence there is less chance for recombination with base region. Hence I_B decreases, α increases.
2. As effective base width decreases minority carrier concentration increases within base. The hole current I_E injected from emitter to Base increases due to this concentration gradient
3. W_B' may be reduced to zero causing voltage breakdown in the transistor. This phenomenon is known as punch through

Q/3 (c) Sketch the transfer curve defined by $I_{DSS} = 12mA$ and $V_P = -6V$

Ans: As $V_P = -6V$, curve is for N channel MOSFET.

To draw a transfer curve of ~~the~~ MOSFET we need atleast four set of point as the curve shape is non linear.

from the given data

$$I_{DSS} = 12mA, \quad V_P = -6V$$

$V_{GS} = 0 \longrightarrow I_{DSS} = 12mA = I_D$

$V_{GS} = V_P = -6V \longrightarrow I = 0mA.$

At $V_{GS} = \frac{V_P}{2} = -3V$

$$I_D = 12mA\left(1 - \frac{-3}{-6}\right)^2$$

$$= 12mA\left(1 - \frac{1}{2}\right)^2$$

$$I_D = \frac{12mA}{4} = 3mA.$$

Shokely equation for drain current

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

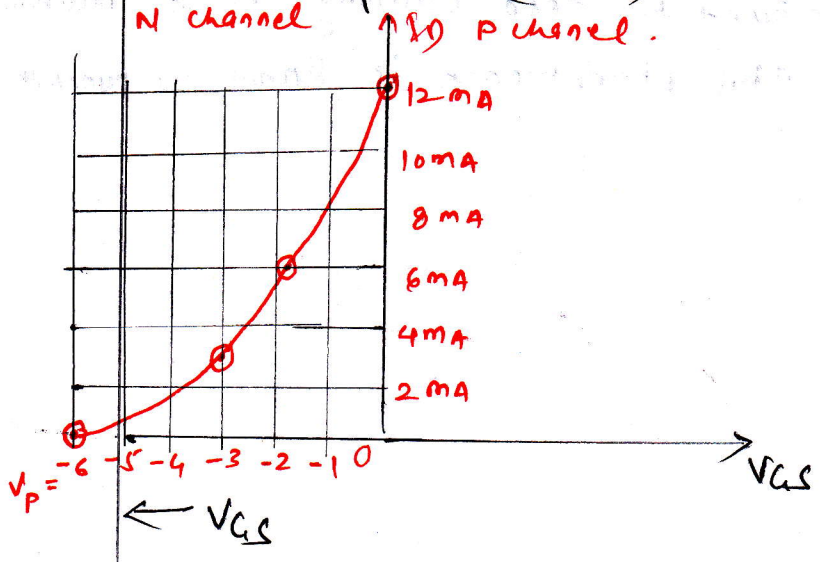
At $I_D = \frac{I_{DSS}}{2} = 6mA$

$$6mA = 12mA\left(1 - \frac{V_{GS}}{V_P}\right)^2 \Rightarrow 1 - \frac{V_{GS}}{V_P} = \frac{1}{\sqrt{2}}$$

$$\frac{V_{GS}}{V_P} = \left(1 - \frac{1}{\sqrt{2}}\right) \Rightarrow V_{GS} = V_P(1 - 0.707)$$

$$= -6(.293)$$

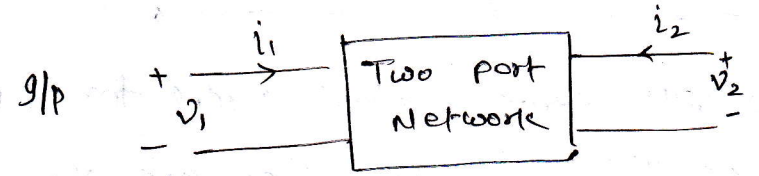
$$= -1.75V$$



V_{GS}	I_D
0	12mA
-1.75	6mA
-3V	2mA
-6V	0mA

9/4 (a) What is the importance of two port networks? How to represent transistor as a hybrid model & derive the model and explain different h parameters.

Ans: Two port devices are specified by two ~~port~~ voltages and two currents. The box below represent two port N/W



We can select two of four quantity as the independent variable and express the other two in terms of chosen independent variables. We can not choose independent parameter arbitrarily as in transformer v_1 and v_2 could not be taken as independent as their ratio is constant now If the current and voltage i_1, v_2 are independent and N/W is linear

$$v_1 = h_{11} i_1 + h_{12} v_2 \quad \text{——} (1)$$

$$i_2 = h_{21} i_1 + h_{22} v_2 \quad \text{——} (2)$$

The quantities $h_{11}, h_{12}, h_{21}, h_{22}$ are called h or hybrid parameters because there dimensions are not all alike.

$h_{11} = \left.\frac{v_1}{i_1}\right|_{v_2=0}$ = Input resistance with O/p shorted

$h_{12} = \left.\frac{v_1}{v_2}\right|_{i_1=0}$ = fraction of O/p voltage at I/p with I/p open circuited, known as reverse open circuit voltage amplification.

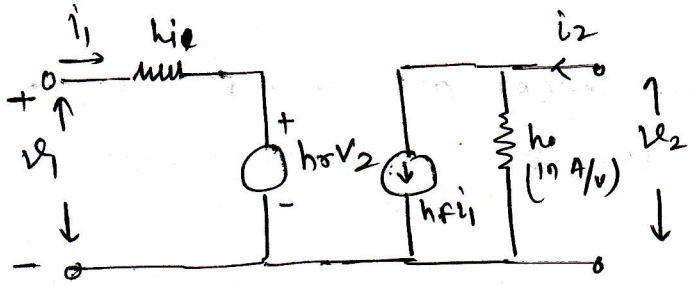
$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2=0}$ = Negative of current gain with O/p shorted.

$h_{22} = \left.\frac{i_2}{v_2}\right|_{i_1=0}$ = Output conductance with I/p open.

i = 11 = I/p, o = 22 = output, f = 21 = forward transfer, r = 21 = reverse transfer.

We will now write h_i, h_o, h_f, h_r in place of h_{11}, h_{22}, h_{12} and h_{21} respectively

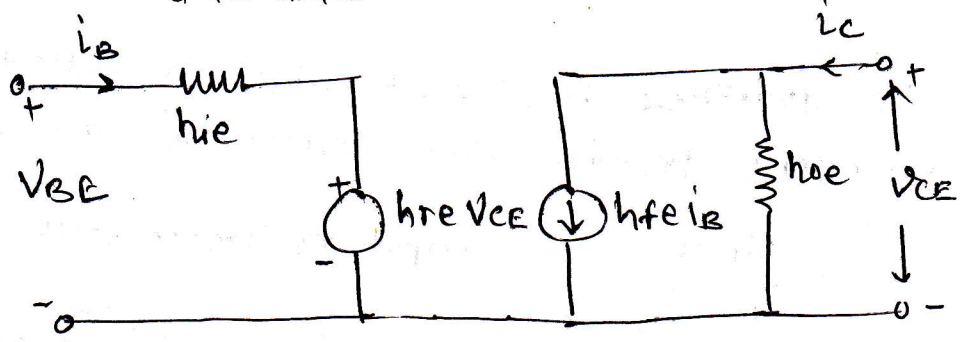
The model may be derived for eq^n (1) and (2) as shown



Now we will derive hybrid model for CE configuration the variables are i_B, i_C, V_{BE} and V_{CE}. Out of these four variable two may be considered as independent. from the characteristics of CE amplifier we know that input ~~voltage~~ current and output voltage may be considered as independent variable and output current and o/p voltage as dependent variable therefore

$$V_{BE} = f_1(i_B, V_{CE})$$
$$i_C = f_2(i_B, V_{CE})$$

Now we will use these variable to draw hybrid model as we have drawn ~~drawn~~



$$V_{BE} = h_{ie} i_B + h_{re} V_{CE}$$
$$i_C = h_{fe} i_B + h_{oe} V_{CE}$$

$$h_{ie} = \left.\frac{V_{BE}}{i_B}\right|_{V_{CE}=0}, \quad h_{re} = \left.\frac{V_{BE}}{V_{CE}}\right|_{i_B=0}, \quad h_{fe} = \left.\frac{i_C}{i_B}\right|_{V_{CE}=0}, \quad h_{oe} = \left.\frac{i_C}{V_{CE}}\right|_{i_B=0}$$

Q/4 (b) The transistor connected in CE config. have $h_{11} = h_i = 1100$, $h_{12} = h_r = 2.5 \times 10^{-4}$, $h_{21} = h_f = 50$, $h_{22} = h_o = 25\,\mu A/V$. If $R_L = 10\,K$ and $R_s = 1K$, find various gains and i/p and output impedances.

Ans:

$$A_I = -\frac{h_{fe}}{1 + h_{oe} R_L} = -\frac{50}{1 + (25 \times 10^{-6} \times 10 \times 10^3)}$$

$$= -40$$

$$A_V = \frac{A_I R_L}{R_i} = -40 \times \frac{10}{1} = \boxed{-400}$$

$$R_i = h_{ie} + h_{re} A_I R_L$$

$$= 1100 + (2.5 \times 10^{-4} \times (-40) \times 10 \times 10^3)$$

$$= \boxed{1000\ \Omega}$$

$$A_{Vs} = \frac{A_V R_i}{R_i + R_s} = -\frac{400 \times 1}{1+1} = \boxed{-200}$$

$$A_{Is} = \frac{A_I R_s}{R_i + R_s} = -\frac{40 \times 1}{1+1} = \boxed{-20}$$

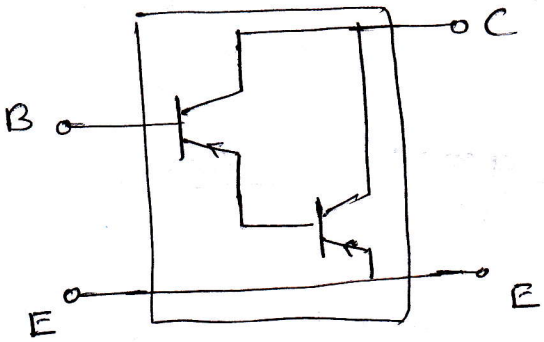
$$Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s}$$

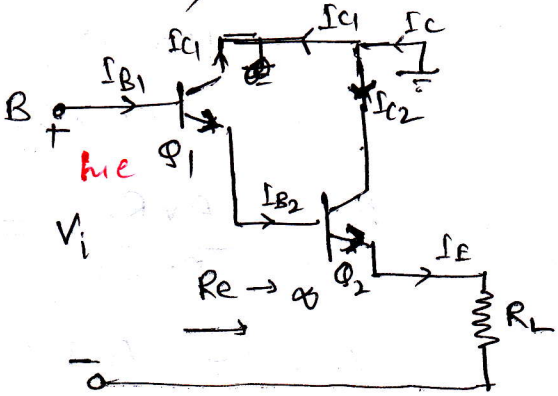
$$= 25 \times 10^{-6} - \frac{50 \times 2.5 \times 10^{-4}}{1100 + 1000} = \boxed{19\,\mu A/V}$$

$$Z_o = \frac{1}{Y_o} = \frac{1}{19\mu} = \boxed{52.6\,K\Omega}$$

Q|4(c) Draw a darlington emitter follower. Also explain why the input impedance is higher than that of single stage emitter follower.

Ans: In some application there is a need for an amplifier with high input impedance. For R_i impedance smaller than about 50K, the emitter follower is satisfactory. To achieve larger input impedance the circuit called the darlington connection is used. The two transistor form a composite pair, the R_i impedance of second transistor constitute the emitter load for the first. The darlington circuit consist of two cascaded emitter followers with infinite emitter resistance seen by the first stage.





The pair can be fabricated in one chip or two transistor may be connected as shown above to make daslington pair. The emitter current of the first transistor drives the second transistor. Therefore the overall current gain increases,

$$I_C = I_{C1} + I_{C2} = \beta_1 I_B + \beta_2 I_{E1}$$

(β_1, β_2 are gain of Q_1 & Q_2)

$$= \beta_1 I_B + \beta_2 (I_B + \beta_1 I_B)$$

$$= \beta_1 I_B + \beta_2 I_B + \beta_1 \beta_2 I_B$$

$$I_C = (\beta_1 + \beta_2 + \beta_1 \beta_2) I_B$$

$$\frac{I_C}{I_B} = \text{current gain of darlington pair}$$

$$= \beta_1 + \beta_2 + \beta_1 \beta_2$$

If $\beta_1 = \beta_2 = 20$.

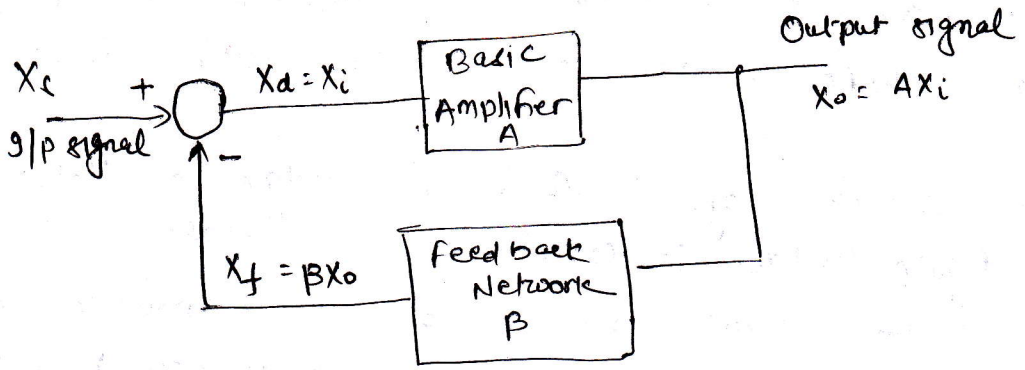
overall gain $\beta = 20 + 20 + 20 \times 20 = 440$.

Darlington pair is high gain high R_i impedance amplifier

8/5: (a) State the three fundamental assumption which are made in order that the expression $A_f = A/(1+AB)$ be satisfied exactly.

Ans

Any one of the o/p connection may be combined with any of the input connections to form feedback amplifier as shown



$$X_d = X_s - X_f = X_i$$

$$\beta = \frac{X_f}{X_o}, \quad A = \frac{X_o}{X_i}$$

With feedback

$$A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f} = \frac{X_o/X_i}{1 + \frac{X_f}{X_i}} = \frac{A}{1 + \frac{X_f}{X_o}\cdot\frac{X_o}{X_i}}$$

$$\boxed{A_f = \frac{A}{1+\beta A}} \quad \text{— (1)}$$

Three conditions must be satisfied for the feedback N/W shown above and eq^n (1) to be true.

(1) The i/p signal is transmitted from amplifier A only towards the o/p not through feedback N/W. If A is deactivated i.e. $A = 0$, output must be zero. Approximately valid under practical conditions.

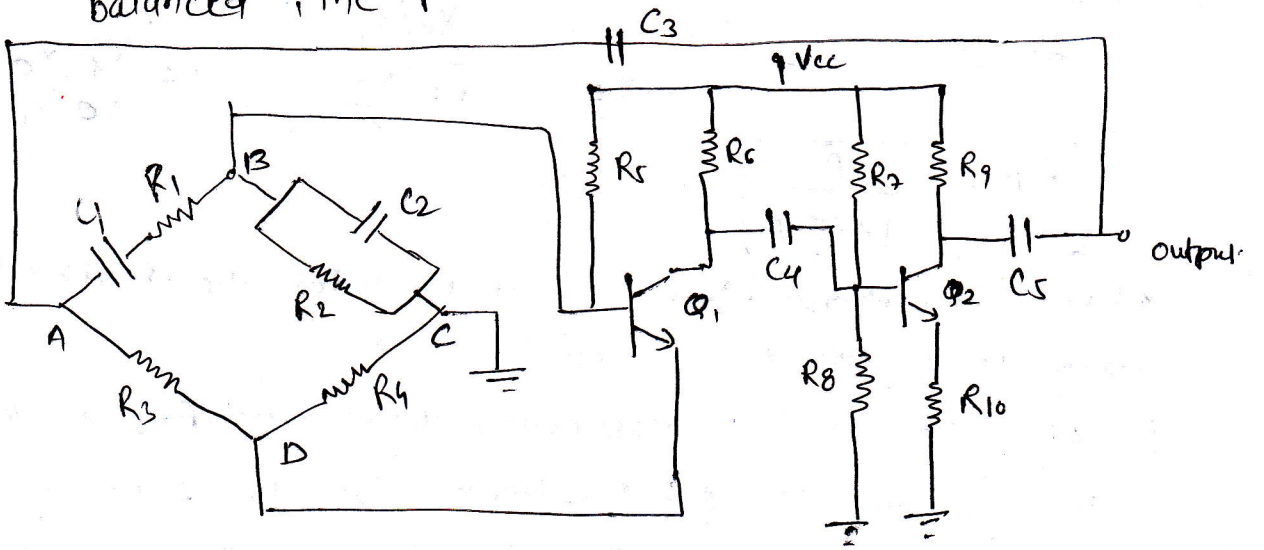
(2) The feedback signal is transmitted from output to input through the β block and not through the amplifier i.e. similar to β network. Amplifier A is unilateral from i/p to o/p and reverse transmission is zero.

(3) The reverse transmission factor β of the feedback N/W is independent of the load and source resistance R_L and R_s and made up of only passive elements (mainly resistors).

Q/5 (b) Sketch the circuit of a Wien bridge oscillator. Determine the frequency of oscillation.

Ans:- Wien bridge is one of most popular oscillator used at frequency range of 20 - 20KHz. This type of oscillator is simple in design, compact in size and provide stable frequency. It employs two transistor each producing a phase shift of 180° and thus producing a total phase shift of 360° or 0°

The circuit diagram of Wien bridge oscillator is shown in figure below. It consist of two stage amplifier with RC bridge circuit. RC bridge circuit provides phase shift for high as well as for low frequency but at one of the intermediate frequency at which Wien bridge is balanced, the phase shift of the bridge becomes 0°.



In the bridge circuit R_1 in series with C_1, R_3, R_4 and R_2 in parallel with C_2 form the four arm.

Oscillator oscillates at frequency for which brige provides zero phase shift

$$R_3\left(\frac{R_2}{1+j\omega C_2R_2}\right) = R_4\left(R_1 - \frac{j}{\omega C_1}\right)$$

$$R_2R_3 = R_4(1+j\omega C_2R_2)\left(R_1 - \frac{j}{\omega C_1}\right)$$

$$R_2R_3 - R_4R_1 - \frac{C_2}{C_1}R_2R_4 + j\frac{R_4}{\omega C_1} - j\omega C_2R_2R_1R_4 = 0$$

separating real and imaginary part.

$$R_2R_3 - R_4R_1 - \frac{C_2}{C_1}R_2R_4 = 0 \Rightarrow \boxed{\frac{C_2}{C_1} = \frac{R_3}{R_4} - \frac{R_1}{R_2}}$$

$$\frac{R_4}{\omega C_1} - \omega C_2 R_2 R_1 R_4 = 0$$

$$\omega^2 = \frac{1}{C_1 C_2 R_1 R_2} \Rightarrow \omega = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}$$

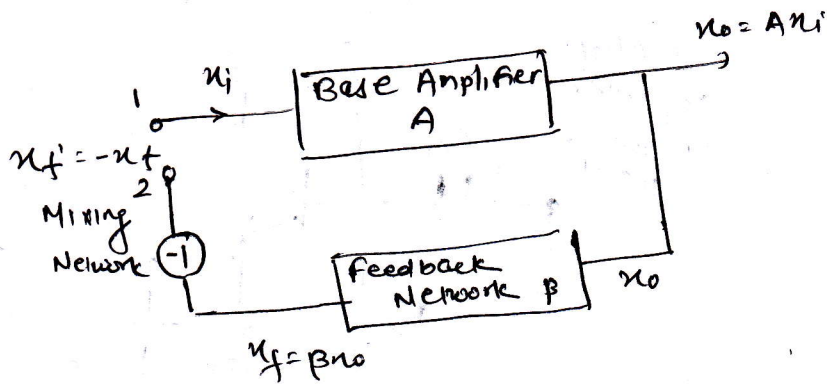
$$f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

If $C_1 = C_2 = C$, $R_1 = R_2 = R$

$$\boxed{f = \frac{1}{2\pi RC}}$$

Q/5 (c) Sketch the circuit diagram for general form of oscillator circuit. Also draw Hartley oscillator and explain its operation.

Ans: Figure below shows an amplifier, a feedback Network and an input mixing network not yet connected to form a closed loop

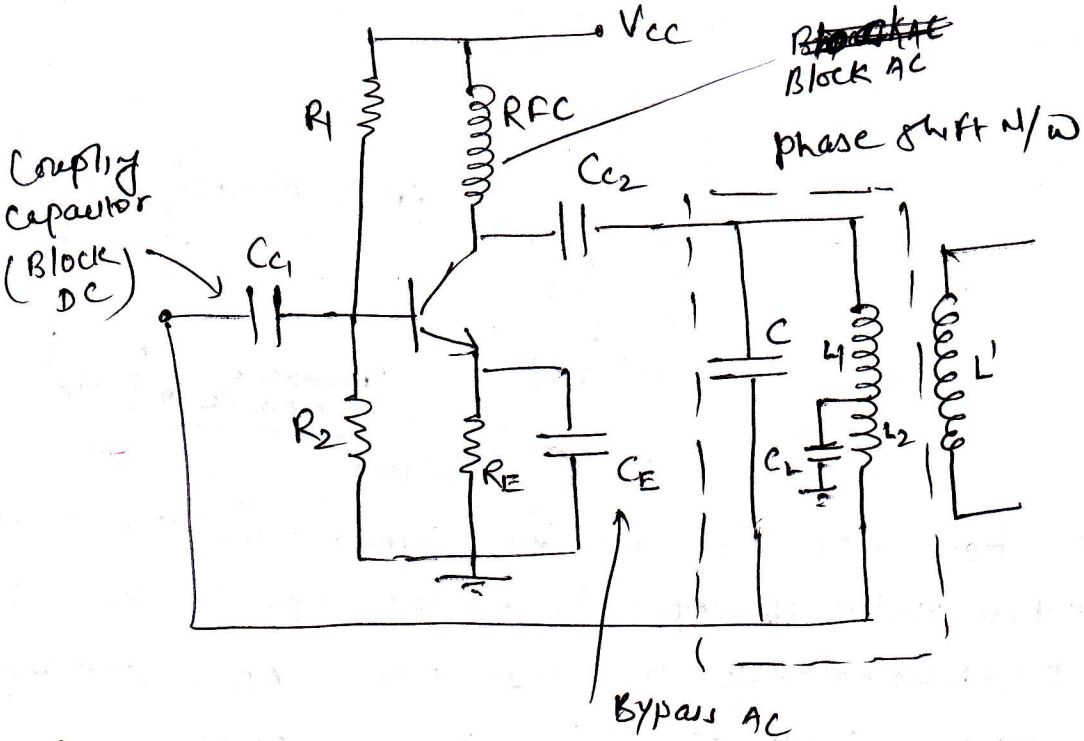


The base amplifier provides output signal x_o which is amplified version of input x_i as the input is x_i. The output of feedback Network is $x_f = \beta x_o = A\beta x_i$ and the o/p of mixing network is $x_f' = -x_f = -A\beta x_i$

Suppose that feedback network and base amplifier parameters are adjusted such that x_f' is exactly equal to x_i and now base amplifier is connected to this feedback signal $x_f' = x_i$ and signal source x_i is disconnected i.e. if terminal 2 is connected to base amplifier, the amplifier would continue to provide same o/p signal x_o as before. The condition $x_f' = x_i$ and $-A\beta = 1$ are needed to determine

freq of oscillation. The diagram drawn is known as general form of oscillator circuit.

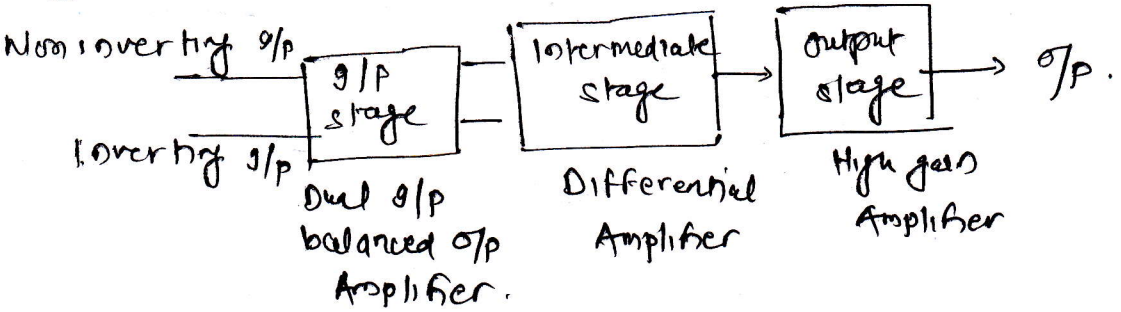
Above concept of feedback and condition $-A\beta = 1$ which is known as barkhausen criterion are used to design oscillator circuits. The signal fed back from o/p to i/p should not have any phase difference i.e. either phase difference should be 0 or multiple of 2π. Hartley oscillator circuit is drawn below which uses only one transistor amplifier which provides 180° of phase shift. rest 180° phase shift needed to have phase shift 360° or to follow barkhausen criterion is provided by feedback network.



The output of the amplifier is given to LC tank circuit which is having one capacitor and two inductor. The voltage across inductor L_2 forms feedback voltage. L_1 or L_2 can not be grounded directly i.e. why capacitor C_2 is used. The feedback network provide 180° of phase shift to the amplified and inverted output of amplifier, total phase shift is now 360. and above circuit oscillate at resonant freq of tank circuit given by $f = \frac{1}{2\pi\sqrt{C(L_1+L_2+2M)}}$

Ans ⑥ ⑨ Draw schematic block diagram of the basic OPAMP with inverting and non inverting inputs. Also indicate its equivalent circuit.

Ans. The schematic block diagram of basic OPAMP is as shown

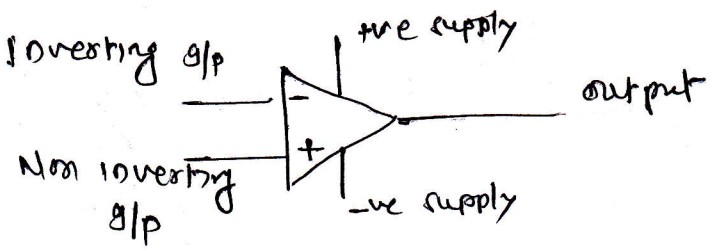


Schematic symbol

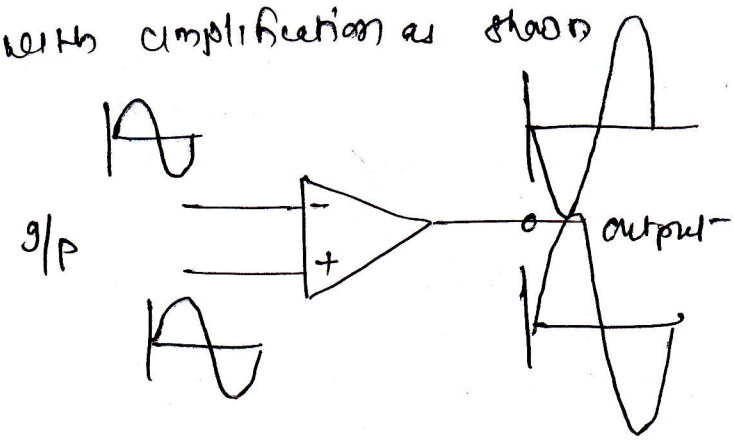
The schematic symbol of an OPAMP is shown below. A is the voltage gain, v_1 is non inverting input and v_2 is inverting input. The differential output is

$$v_{in} \text{ or } v_d = v_1 - v_2$$

$$v_{out} = A v_{in} = A(v_1 - v_2)$$

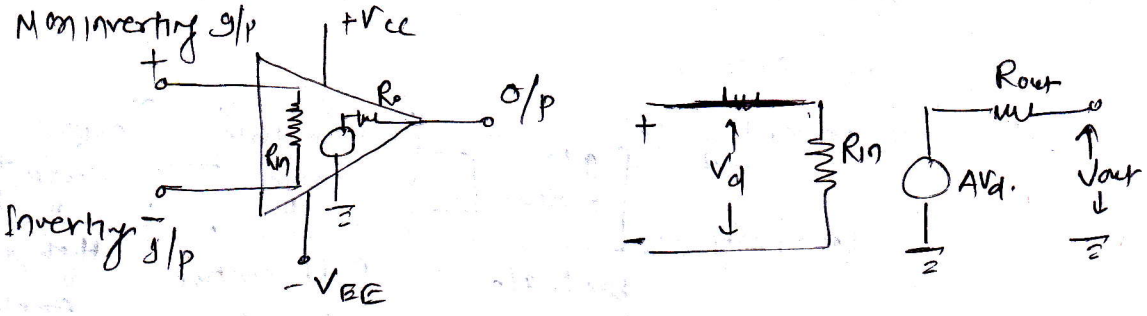


The terminal marked +ve is non inverting input and terminal marked -ve is inverting input of OPAMP. A signal applied at +ve terminal appears with same polarity and amplified at the output. while an input applied to -ve input terminals appear at the output with opposite polarity and with amplification as shown



Equivalent Circuit of an OPAMP.

Figure shows an OPAMP equivalent circuit which is useful in analyzing basic OPAMP



$$V_{out} = A V_d = A(V_1 - V_2)$$

A is large signal voltage gain, V_d is differential input voltage V_1 and V_2 are the input voltages at non inverting and inverting terminals respectively.

Q/6 (b) The data sheet of an OPAMP gives the typical values of $A_{DM} = 200000$ and CMRR = 90 dB. What will be the common mode voltage gain.

Ans.

$$CMRR = \frac{A_{dM}}{A_{CM}}$$

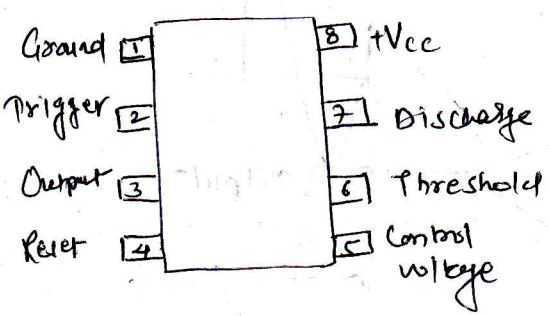
$$20 \log_{10} CMRR = 20 \log_{10} \left(\frac{A_{dM}}{A_{CM}} \right) \quad \text{(in dB)}$$

$$90 = 20 \log_{10} \left(\frac{200000}{A_{CM}} \right)$$

$$\boxed{A_{CM} = 6.324}$$

Q/7 (c) Explain 555 Timer IC its operation and output waveform that can be obtained in astable mode of operation.

Ans: The 555 IC is available as an 8 pin metal as shown



PIN 1 : Grounded Terminal
All voltages are measured wrt to this terminal.

pin 2 : Trigger — Inverting input terminal of OPAMP.

pin 3 : Output — Output of timer is available in this pin. ground.

pin 4 : Reset — To disable or reset the timer a reset a negative pulse is applied to this pin.

pin 5 : Control voltage — To control threshold and trigger levels this pin is used.

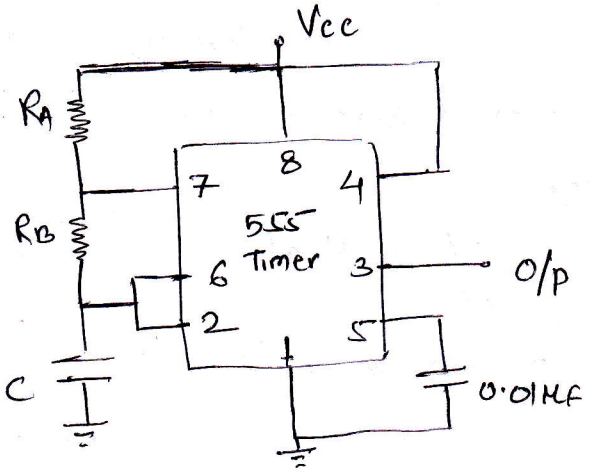
pin 6 : Threshold — This is non inverting input of comparator 1.

pin 7 : Discharge — This terminal is connected to collector of transistor and mostly a capacitor is connected between this terminal and gnd.

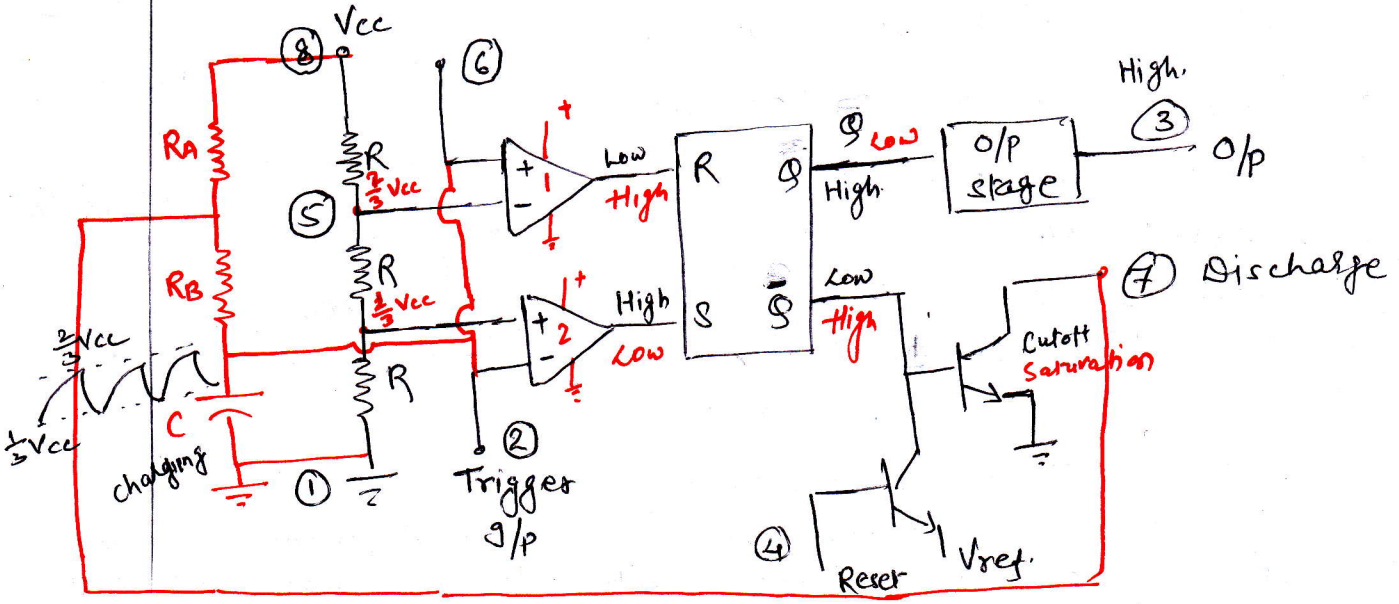
pin 8 : Supply — Supply voltage of 5V to 18V is applied here

Timer 555 as an astable multivibrator

Multivibrator is a switching circuit and may be defined as an electronic circuit that generates non sinusoidal waves such as square, square wave etc. Now we will see use of 555 timer IC in astable mode. Circuit connection is as shown



Internal Circuit of 555 timer is as shown



Operation of astable multivibrator

In the circuit diagram capacitor is connected via to V_{cc} via R_A and R_B. Comparator 1 have inverting terminal fixed to $\frac{2}{3}V_{cc}$ and comparator 2 have non inverting terminal fixed to $\frac{1}{3}V_{cc}$. Now when switch is on, capacitor will start charging via R_A and R_B. when capacitor charge is below $\frac{1}{3}V_{cc}$ comparator 1 output will be low and comparator 2 output will also be ~~high~~ Low which makes $R=0$ and $S=1$ to the flip flop i.e. $S=0$ and $\bar{S}=1$. Hence o/p is 1.

output Q is high i.e. 1 and $\bar{Q}=0$ which drives the discharge transistor to cut off and capacitor keeps on charging via R_A and R_B.

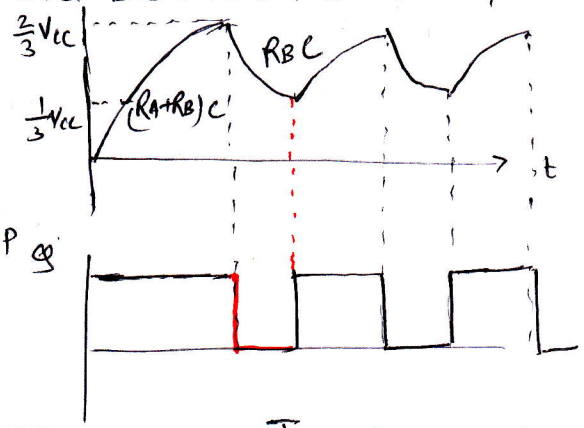
when capacitor charges reached $\frac{1}{3}V_{cc}$ and rising

comparator 1 output will be Low

comparator 2 output will be High

i.e. $R=0$, $S=1$, same output will be there i.e. $Q=1$, $\bar{Q}=0$

capacitor keeps on charging



when capacitor charge is $\frac{2}{3}V_{cc}$ and rising

comparator 1 o/p → High

comparator 2 o/p → Low

$R=1$, $S=0$ $\Rightarrow Q=0$, $\bar{Q}=1$

$\bar{Q}=1$ drives the transistor into saturation and capacitor is now grounded via pin 7 through R_B and started discharging.

As charge of capacitor reaches again $\frac{1}{2}V_{cc}$ and decreasing

comparator 1 o/p → Low

comparator 2 o/p → High

$R=0$, $S=1$ $\Rightarrow Q=1$, $\bar{Q}=0$

transistor will be in cutoff again

and capacitor starts charging again

$T_{HIGH} = 0.693 (R_A+R_B)C$

$T_{Low} = 0.693\ R_BC$

$T = 0.693 (R_A+2R_B)C$

$f = \frac{1}{T} = \frac{1}{0.693(R_A+2R_B)C}$

$$\boxed{f = \frac{1.44}{(R_A+2R_B)C}}$$

and we get pulse waveform at o/p. and this circuit is known as free running multivibrator. both states are quasistable states.